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EXAMINER	
PERSINO, RAYMOND B	

ART UNIT	PAPER NUMBER
2682	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,868	DUNWORTH ET AL.	
	Examiner	Art Unit	
	Raymond B. Persino	2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/6/02 & 11/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 6, 7, 26, 30 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by NELSON et al (US 2002/0075080 A1).

Regarding claim 1, NELSON et al discloses a method comprising: detecting an amplitude of an oscillator signal generated by an oscillator during a calibration mode (56 of figure 6) in which a phase lock loop is disabled (see from 66 of figure 6 that loop was not connected during calibration); comparing the detected amplitude (62 of figure 6) to a target amplitude; and adjusting (70 of figure 6) the oscillator based on the comparison (see figure 6 and paragraphs 30-37).

Regarding claim 2, see the rejection of the parent claim concerning the subject matter this claim depends from. NELSON et al further discloses enabling a phase locked loop to control frequency of the oscillator after adjusting the oscillator (see 66 and 68 of figure 6 and paragraphs 30-37).

Regarding claim 3, see the rejection of the parent claim concerning the subject matter this claim depends from. NELSON et al further discloses that the oscillator comprises a voltage controlled oscillator with a configurable tail current source, wherein detecting the amplitude comprises detecting an output voltage amplitude of the VCO, and wherein adjusting the oscillator comprises adjusting the configurable tail current source to achieve a desired output voltage amplitude (paragraphs 19 and 25 and 28-29). Note that an alternative rejection based upon 35 U.S.C. 103 is provided below.

Regarding claim 6, see the rejection of the parent claim concerning the subject matter this claim depends from. NELSON et al further discloses selecting the desired target amplitude based on an operation mode of a wireless communication device implementing the oscillator (paragraphs 19 and 36).

Regarding claim 7, see the rejection of the parent claim concerning the subject matter this claim depends from. NELSON et al further discloses adjusting discrete circuitry of the oscillator that affects a frequency of the oscillator prior to enabling a phase locked loop (58 of figure 6).

Regarding claim 26, NELSON et al discloses an apparatus comprising: circuitry that detects a signal amplitude of an oscillator for an input parameter prior to enabling a phase locked; and circuitry that adjusts the oscillator to achieve a desired signal amplitude (see figure 6 and paragraphs 30-37).

Regarding claim 30, see the rejection of the parent claim concerning the subject matter this claim depends from. NELSON et al further discloses circuitry that calibrates a signal frequency of the oscillator; and circuitry that enables the phase locked loop

after adjusting the oscillator to achieve a desired signal amplitude and after calibrating the signal frequency of the oscillator (58 of figure 6).

Regarding claim 34, see the rejection of the parent claim concerning the subject matter this claim depends from. NELSON et al further discloses a frequency synthesizer comprising: an oscillator; means for disabling a phase locked loop of an oscillator; means for detecting a signal amplitude of the oscillator for an input parameter when the phase locked loop is disabled; and means for adjusting the oscillator to achieve a desired signal amplitude (see figure 6 and paragraphs 30-37).

3. Claims 9, 10, 17, 18, 31, 32, 36, 37 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by ROGERS (US 6,680,655 B2).

Regarding claim 9, ROGERS discloses a method of calibrating an amplitude of an oscillator (column 4 line 36 to column 6 line 63) comprising: setting a configurable tail current source of the oscillator to a maximum current setting; and reducing the current setting of the configurable tail current source (column 7 lines 21-25) in discrete steps until the amplitude of the oscillator would fall below a target (column 8 line 55 to column 9 line 11).

Regarding claim 10, see the rejection of the parent claim concerning the subject matter this claim depends from. ROGERS further discloses reducing the current setting of the configurable tail current source in discrete steps comprises de-activating switched unit current sources in discrete steps (column 8 line 55 to column 9 line 11).

Regarding claim 17, ROGERS discloses a frequency synthesizer comprising: an oscillator (column 4 line 36 to column 6 line 63) including a configurable tail current

source (column 7 lines 21-25); circuitry that sets the configurable tail current source of the oscillator to a maximum current setting; and circuitry that reduces the current setting of the configurable tail current source in discrete steps until an oscillating signal of the oscillator is below a target (column 8 line 55 to column 9 line 11).

Regarding claim 18, see the rejection of the parent claim concerning the subject matter this claim depends from. ROGERS further discloses that the circuitry that reduces the current setting reduces the current setting in discrete steps by de-activating switched unit current sources in discrete steps (column 8 line 55 to column 9 line 11).

Regarding claim 31, ROGERS discloses an apparatus comprising: circuitry that sets a configurable tail current source of an oscillator to a maximum current setting; and circuitry that reduces the current setting of the configurable tail current source in discrete steps until an amplitude of an oscillating signal of the oscillator is below a target (column 4 line 36 to column 6 line 63, column 7 lines 21-25, and column 8 line 55 to column 9 line 11).

Regarding claim 32, see the rejection of the parent claim concerning the subject matter this claim depends from. ROGERS further discloses that the configurable tail current source includes a set of switched unit current sources, wherein the circuitry that reduces the current setting of the adjustable tail current source in discrete steps de-activates the switched unit current sources in discrete steps. (column 8 line 55 to column 9 line 11).

Regarding claim 36, ROGERS discloses a frequency synthesizer comprising: an oscillator including a configurable tail current source; means for setting the configurable

tail current source of the oscillator to a maximum current setting; and means for reducing the current setting of the configurable tail current source in discrete steps until an amplitude of a signal of the oscillator would be below a target (column 4 line 36 to column 6 line 63, column 7 lines 21-25, and column 8 line 55 to column 9 line 11).

Regarding claim 37, see the rejection of the parent claim concerning the subject matter this claim depends from. ROGERS further discloses that the means for reducing comprises a set of switched unit current sources (column 4 line 36 to column 6 line 63 and column 7 lines 21-25).

Regarding claim 39, ROGERS discloses an oscillator comprising: an oscillator tank that generates an oscillating voltage signal; and a configurable tail current source that defines an amplitude of the oscillating voltage signal, wherein the configurable tail current source includes a set of switched unit current sources that can be selectively activated to adjust the amplitude (column 4 line 36 to column 6 line 63 and column 7 lines 21-25).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-5, 8, 12, 13-16, 27, 28 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over NELSON et al (US 2002/0075080 A1) in view of ROGERS (US 6,680,655 B2).

Regarding claim 3, see the rejection of the parent claim concerning the subject matter this claim depends from. It is believed that NELSON et al further discloses that the oscillator comprises a voltage controlled oscillator with a configurable tail current source, wherein detecting the amplitude comprises detecting an output voltage amplitude of the VCO, and wherein adjusting the oscillator comprises adjusting the configurable tail current source to achieve a desired output voltage amplitude. See alternative rejection based upon 35 U.S.C. 102(e) above. However, even if is disagreed that NELSON et al discloses the above subject matter, ROGERS does. ROGERS discloses an oscillator that comprises a voltage controlled oscillator with a configurable tail current source (column 7 lines 21-25), wherein detecting the amplitude comprises detecting an output voltage amplitude of the VCO, and wherein adjusting the oscillator comprises adjusting the configurable tail current source to achieve a desired output voltage amplitude (column 4 line 36 to column 6 line 63). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the voltage detection/correction scheme of ROGERS in the circuit of NELSON et al. ROGERS's detection/correction scheme is advantageous in for use in monolithic implementations since it automatically compensates for variations in load resistance, process parameters and component tolerances without requiring expansive manual adjustments at the board level.

Regarding claim 4, see the rejection of the parent claim concerning the subject matter this claim depends from. ROGERS further discloses that the a tail current source includes a set of switched unit current sources, wherein adjusting the tail current source comprises selectively activating a subset of the switched unit current sources (see Q1-Q6 and 36 in figure 3 and column 4 line 36 to column 6 line 63)

Regarding claim 5, see the rejection of the parent claim concerning the subject matter this claim depends from. ROGERS further discloses selectively activating the subset of the switched unit current sources comprises de-activating switched unit current sources in discrete steps until the output voltage amplitude would fall below the target amplitude (column 8 line 55 to column 9 line 11).

Regarding claim 8, see the rejection of the parent claim concerning the subject matter this claim depends from. However, NELSON et al does not disclose detecting the amplitude comprises generating a DC voltage indicative of the amplitude of an oscillator signal, and wherein comparing the detected amplitude to a target amplitude comprises comparing the generated DC voltage to a target DC voltage. ROGERS discloses detecting the amplitude comprises generating a DC voltage indicative of the amplitude of an oscillator signal, and wherein comparing the detected amplitude to a target amplitude comprises comparing the generated DC voltage to a target DC voltage (column 7 lines 27 to column 8 line 15). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the voltage detection/correction scheme of ROGERS in the circuit of NELSON et al. ROGERS's detection/correction scheme is advantageous in for use in monolithic implementations

since it automatically compensates for variations in load resistance, process parameters and component tolerances without requiring expansive manual adjustments at the board level.

Regarding claim 12, NELSON et al discloses a frequency synthesizer comprising: an oscillator; a phase locked loop that controls a frequency of an oscillating signal of the oscillator; and an amplitude calibration unit that when the phase locked loop is disabled in order to achieve a desired amplitude for the oscillating signal (see figure 6 and paragraphs 30-37). However, NELSON et al does not disclose that the oscillator includes a configurable tail current source and that the amplitude calibration unit calibrates the configurable tail current source. ROGERS discloses that the oscillator includes a configurable tail current source (column 7 lines 21-25) and that the amplitude calibration unit calibrates the configurable tail current source (column 4 line 36 to column 6 line 63). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the voltage detection/correction scheme of ROGERS in the circuit of NELSON et al. ROGERS's detection/correction scheme is advantageous in for use in monolithic implementations since it automatically compensates for variations in load resistance, process parameters and component tolerances without requiring expansive manual adjustments at the board level.

Regarding claim 13, see the rejection of the parent claim concerning the subject matter this claim depends from. ROGERS further discloses the oscillator comprises a voltage controlled oscillator, and the configurable tail current source comprises a number of switched unit current sources, wherein the amplitude calibration unit detects

a voltage amplitude of the oscillator and adjusts the configurable tail current source by activating a subset of the switched unit current sources to achieve the desired voltage amplitude of the oscillator (column 4 line 36 to column 6 line 63 and column 7 lines 21-25).

Regarding claim 14, see the rejection of the parent claim concerning the subject matter this claim depends from. ROGERS further discloses that the amplitude calibration unit activates the subset of switched unit current sources by de-activating switched unit current sources in discrete steps until voltage amplitude of the oscillator would fall below a target (column 8 line 55 to column 9 line 11).

Regarding claim 15, see the rejection of the parent claim concerning the subject matter this claim depends from. NELSON et al further discloses that the frequency synthesizer enables the phase locked loop following calibration of the configurable tail current source. (see 66 and 68 of figure 6 and paragraphs 30-37).

Regarding claim 16, see the rejection of the parent claim concerning the subject matter this claim depends from. NELSON et al further discloses that the oscillator includes additional configurable circuitry that affects the frequency of the oscillator, wherein the frequency synthesizer further comprises a frequency calibration unit that adjusts the additional configurable circuitry of the oscillator to adjust the frequency of the oscillator when the phase locked loop is disabled (58 of figure 6).

Regarding claim 27, see the rejection of the parent claim concerning the subject matter this claim depends from. However, NELSON et al does not discloses that the oscillator comprises a voltage controlled oscillator that includes a configurable tail

current source comprising a set of switched unit current sources, wherein the circuitry that adjusts the oscillator selectively activates a subset of the switched unit current sources to achieve the desired signal amplitude. ROGERS discloses that the oscillator comprises a voltage controlled oscillator that includes a configurable tail current source comprising a set of switched unit current sources, wherein the circuitry that adjusts the oscillator selectively activates a subset of the switched unit current sources to achieve the desired signal amplitude (column 4 line 36 to column 6 line 63 and column 7 lines 21-25). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the voltage detection/correction scheme of ROGERS in the circuit of NELSON et al. ROGERS's detection/correction scheme is advantageous in for use in monolithic implementations since it automatically compensates for variations in load resistance, process parameters and component tolerances without requiring expansive manual adjustments at the board level.

Regarding claim 28, see the rejection of the parent claim concerning the subject matter this claim depends from. However, NELSON et al does not discloses that the circuitry that adjusts the oscillator selectively activates the subset by de-activating switched unit current sources in discrete steps until signal amplitude of the oscillator is below a target. ROGERS discloses that the circuitry that adjusts the oscillator selectively activates the subset by de-activating switched unit current sources in discrete steps until signal amplitude of the oscillator is below a target (column 4 line 36 to column 6 line 63 and column 7 lines 21-25). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the voltage

detection/correction scheme of ROGERS in the circuit of NELSON et al. ROGERS's detection/correction scheme is advantageous in for use in monolithic implementations since it automatically compensates for variations in load resistance, process parameters and component tolerances without requiring expansive manual adjustments at the board level.

Regarding claim 35, see the rejection of the parent claim concerning the subject matter this claim depends from. However, NELSON et al does not discloses that the oscillator includes a configurable tail current source, wherein the means for adjusting comprises a set of switched unit current sources in the tail current source. ROGERS discloses that the oscillator includes a configurable tail current source, wherein the means for adjusting comprises a set of switched unit current sources in the tail current source (column 4 line 36 to column 6 line 63 and column 7 lines 21-25). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the voltage detection/correction scheme of ROGERS in the circuit of NELSON et al. ROGERS's detection/correction scheme is advantageous in for use in monolithic implementations since it automatically compensates for variations in load resistance, process parameters and component tolerances without requiring expansive manual adjustments at the board level.

6. Claims 11, 19, 33 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over ROGERS (US 6,680,655 B2) in view of POPE (US 6,163,228 A).

Regarding claim 11, see the rejection of the parent claim concerning the subject matter this claim depends from. However, ROGERS does not disclose selecting the

target based on a mode of operation of a wireless communication device implementing the oscillator. POPE discloses selecting the target based on a mode of operation of a wireless communication device implementing the oscillator (column 1 lines 51-62). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the VCO mode adjustment of POPE. This would result in reduced power consumption thus extending battery life of wireless devices.

Regarding claim 19, see the rejection of the parent claim concerning the subject matter this claim depends from. However, ROGERS does not disclose circuitry that selects the target based on a mode of operation of a wireless communication device implementing the oscillator. POPE discloses selecting the target based on a mode of operation of a wireless communication device implementing the oscillator (column 1 lines 51-62). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the VCO mode adjustment of POPE. This would result in reduced power consumption thus extending battery life of wireless devices.

Regarding claim 33, see the rejection of the parent claim concerning the subject matter this claim depends from. However, ROGERS does not disclose circuitry that selects the target based on a mode of operation of a wireless communication device implementing the apparatus. POPE discloses circuitry that selects the target based on a mode of operation of a wireless communication device implementing the apparatus. (column 1 lines 51-62). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the VCO mode adjustment of

POPE. This would result in reduced power consumption thus extending battery life of wireless devices.

Regarding claim 38, see the rejection of the parent claim concerning the subject matter this claim depends from. However, ROGERS does not disclose means for selecting the target based on a mode of operation of a wireless communication device implementing the frequency synthesizer. POPE discloses means for selecting the target based on a mode of operation of a wireless communication device implementing the frequency synthesizer (column 1 lines 51-62). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the VCO mode adjustment of POPE. This would result in reduced power consumption thus extending battery life of wireless devices.

7. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over NELSON et al (US 2002/0075080 A1) in view of ROGERS (US 6,680,655 B2) and further in view of the applicant admitted prior art.

Regarding claim 20, NELSON et al discloses a frequency synthesizer that generates waveforms, wherein the frequency synthesizer comprises an oscillator, a phase locked loop that controls a frequency of an oscillating signal of the oscillator, and an amplitude calibration unit that calibrates when the phase locked loop is disabled in order to achieve a desired amplitude of the oscillating signal (see figure 6 and paragraphs 30-37). However, NELSON et al does not disclose that the oscillator including a configurable tail current source and that the amplitude calibration unit calibrates the configurable tail current source; and a mixer that mixes the waveforms.

ROGERS discloses that the oscillator includes a configurable tail current source (column 7 lines 21-25) and that the amplitude calibration unit calibrates the configurable tail current source (column 4 line 36 to column 6 line 63). However, ROGERS does not disclose a mixer that mixes the waveforms. Included in the applicant's admitted prior art is the fact that frequency synthesizers send a waveform to a mixer that mixes the waveforms (pages 1 and 2 of the applicant's specification). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the voltage detection/correction scheme of ROGERS in the circuit of NELSON et al and for the frequency synthesizers send a waveform to a mixer. ROGERS's detection/correction scheme is advantageous in for use in monolithic implementations since it automatically compensates for variations in load resistance, process parameters and component tolerances without requiring expansive manual adjustments at the board level. Having a mixer that receives waveforms from frequency synthesizers allows information to be sent and received at desired radio frequencies. This is beneficial in that information can simultaneously be sent at different frequencies thus increasing that amount of information that can be sent at a given time.

Regarding claim 21, see the rejection of the parent claim concerning the subject matter this claim depends from. The applicant's admitted prior art further discloses a receiver that receives RF waveforms, wherein the mixer down-mixes the received RF waveforms to a baseband signal using the waveforms generated by the frequency synthesizer as a timing reference (pages 1 and 2 of the applicant's specification).

Regarding claim 22, see the rejection of the parent claim concerning the subject matter this claim depends from. The applicant's admitted prior art further discloses a transmitter that transmits the waveforms, wherein the mixer modulates baseband signals into the waveforms prior to transmission (pages 1 and 2 of the applicant's specification).

8. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over ROGERS (US 6,680,655 B2) in view of the applicant admitted prior art.

Regarding claim 23, ROGERS discloses a frequency synthesizer comprising: an oscillator (column 4 line 36 to column 6 line 63) including a configurable tail current source (column 7 lines 21-25); circuitry that sets the configurable tail current source of the oscillator to a maximum current setting; and circuitry that reduces the current setting of the configurable tail current source in discrete steps until an oscillating signal of the oscillator is below a target (column 8 line 55 to column 9 line 11). However, ROGERS does not disclose a mixer that mixes the waveforms. Included in the applicant's admitted prior art is the fact that frequency synthesizers send a waveform to a mixer that mixes the waveforms (pages 1 and 2 of the applicant's specification). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a frequency synthesizer to send a waveform to a mixer. Having a mixer that receives waveforms from frequency synthesizers allows information to be sent and received at desired radio frequencies. This is beneficial in that information can simultaneously be sent at different frequencies thus increasing that amount of information that can be sent at a given time.

Regarding claim 24, see the rejection of the parent claim concerning the subject matter this claim depends from. The applicant's admitted prior art further discloses a receiver that receives RF waveforms, wherein the mixer down-mixes the received RF waveforms to a baseband signal using the waveforms generated by the frequency synthesizer as a timing reference (pages 1 and 2 of the applicant's specification).

Regarding claim 25, see the rejection of the parent claim concerning the subject matter this claim depends from. The applicant's admitted prior art further discloses a transmitter that transmits the waveforms, wherein the mixer modulates baseband signals into the waveforms prior to transmission (pages 1 and 2 of the applicant's specification).

9. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over NELSON et al (US 2002/0075080 A1) in view of ROGERS (US 6,680,655 B2) and further in view of POPE (US 6,163,228 A).

Regarding claim 29, see the rejection of the parent claim concerning the subject matter this claim depends from. However, neither NELSON et al nor ROGERS disclose circuitry that selects the desired signal amplitude based on an operation mode of a wireless communication device implementing the oscillator. POPE discloses circuitry that selects the desired signal amplitude based on an operation mode of a wireless communication device implementing the oscillator. (column 1 lines 51-62). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the VCO mode adjustment of POPE. This would result in reduced power consumption thus extending battery life of wireless devices.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

JONES (US 6,653,908 B1)

ROTZOLL et al (US 5,625,325 A)

DUNWORTH et al (US 2003/0171105 A1)

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Raymond B. Persino whose telephone number is (703) 308-7528. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian C. Chin can be reached on (703) 308-6739. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Raymond B. Persino RP

Examiner
Art Unit 2682

RP

LEE NGUYEN
PRIMARY EXAMINER